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Evaluating the Performance of Unified Power Flow Controller (UPFC) On Fault Current Limitation in the Nigrian 330kv Power System.

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Abstract: *The Performance of Unified Power Flow Controller (UPFC) on Fault Current Limitation in a 330kV Power Network. The SIMULINK model of the Nigerian 330kV system was developed and the model of the UPFC was developed and integrated into the power system model. Results from simulation carried out showed the versatility of the UPFC in the protective limitation of excessive fault current in the system. Evaluation carried out indicated that the UPFC achieved an effective average of 59.23% fault current limitation. This result was shown to have high impact for the protection of critical assets within the power system such as circuit breakers. At a fault impedance of 0.0001Ω, the UPFC provided a 45.81% protection margin for the type of high voltage circuit breakers used on the 330kV system. Apart from interrupting capacity of circuit breakers, this action of the UPFC would also help to increase the life expectancy of circuit breaker contacts between overhaul.*

Keywords: *Unified Power flow controller, Fault Current, Protection and Limitation.*

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I. Introduction

In modern power system, the increasing rate of energy demand pushes the increase in the addition of more generation and transmission system to the grid. As an unwelcome consequences of this, fault currents are day-to-day increasing [1]. Many utilities all over the world are experiencing the problem of astonishing short circuit current (fault current) levels [1]. A fault is an unintentional short circuit, or partial short-circuit, in an electric circuit. Faults on power system are inevitable due to external or internal causes, lightning may strike the over head lines causing insulation damage, incidences of downed or crossed power lines cause faults. During a fault, excessive current called fault current flows high and may exceed ten times the rated current of a piece of plant [2].

Millions of dollars are spent each year to maintain and protect power grids from potentially destructive fault currents [3]. These large currents can damage or degrade circuit breakers and other expensive transmission and distribution components. It is well established that the fault current levels in a network increases proportionally with the addition of lines and new generation [1]. This happens to be the case with the Nigerian 330kV system, especially considering the addition of transmission and generation components to it as a result of the National Integrated Power project (NIPP). This fact means that the short-circuit current rating (i.e the fault current withstand) of existing transmission assets on the Nigerian 330kV system will be exceeded. Increasing rate of fault current levels on power systems cause undesired consequences which may be summarized as follows[1]:

- Equipment is exposed to unacceptable thermal stresses;
- Equipment is exposed to unacceptable electro-dynamic forces;
- Short circuit breaking capability of high voltage circuit breakers are typically limited to 80kA[4];
- In order to prevent equipment damage, faster circuits breakers are required. This requirement faces both technical and economical restrictions.
- Step and touch voltages are also increased as a result of increasing short circuit levels. This will cause safety problems to the personnel;
- Switching over voltage transients will become more severe, due to significant short circuit currents.

These problems put more pressure on power system protection equipment and their configuration. Furthermore the fault clearing time of conventional protection system (Relay/Circuit breaker) is not instantaneous, for it depends on the operating time settings of the over current relay and the circuit breakers tripping time, hence a system that can swing faster into action to limit the destructive effects of the fault current is necessary.

Due to the above-mentioned problems, the subject of fault current level reduction has gained a considerable attention in recent years among electric utilities[5]. The idea behind this line of protection research is to reduce the stress within the network or limit the stress over certain assets (e.g the circuit breaker itself). A number of fault current limitation techniques have been introduced in the iterative. Some of this protection techniques include super conducting fault current limiter [6][7], HVDC links [8] and current limiting reactor [9] [10]. The super conducting fault current limiters use superconducting material such as NbT and MgB_2 to transfer from superconducting state to the normal state, if exposed to high current levels. Although this limiter seems to be an ideal fault current limiter, it is still too expensive, especially due to the cost of its complicated cryogenic system. HVDC links are used to diminish inter-area short circuit current. However, it is reported that this method is not economically justified. Among the excessive fault current limiting methods indicated, the current limiting reactor is argued to be the most practical approach. However it is reported [11] that current reactor may degrade both voltage stability and transient stability of the power system. Consequently a more versatile protection technique becomes necessary. Such a technique should possess almost instantaneous response to fault and have dynamic and enhanced power control capability. Flexible AC Transmission System (FACTS) devices fit into this requirement. The speed, the power transfer and control capabilities of FACTS can be applied to enhance the protection of the Nigerian 330kV transmission system from destructive over current. The problem investigated in this work is the application of the Unified Power Flow Controller (UPFC) to enhance the protection of the Nigerian 330kV power system by effectively limiting destructive fault current.

Hence the paper covers application of the power transfer and control capability of FACTS devices for the protection of the 330kV system from excessive fault current. It includes the MATLAB model of the unified power flow controller, the 330kV system and the fault current limitation analysis of the FACTS devices within power systems. However, it does not include compensating for the impact of FACTS dynamics on the operation of protection relays within the network.

II. Flexible AC Transmission System (FACTS)

Flexible Alternating Current Transmission Systems (FACTS), according to IEEE definition are "Alternating current transmission systems incorporating power electronic based and other static controllers to enhance controllability and increase power transfer capability [12]. Most of the publications on FACTS stress the point that FACTS are used to improve a power system performance by modifying the transmission line parameters.

Literature survey indicates, what is most interesting for power transmission planners is that FACTS technology opens up new opportunities for controlling power and enhancing the usable capacity of present, as well as new and upgraded lines [13]. The possibility that current through a line can be controlled at a reasonable cost enables a large potential of increasing the capacity of existing line with larger conductors, and use of one of the FACTS controllers to enable corresponding power to flow through such lines under normal and contingency conditions.

It is reported in the literature [14][15] that these opportunities arise through the ability of FACTS controllers to control the interrelated parameters that govern the operation of transmission systems including series impedance, shunt impedance, current, voltage, phase angle, and the damping of oscillations at various frequencies below the rated frequency. These constraints cannot be overcome, while maintaining the required system reliability, by mechanical means without lowering the useable transmission capacity. The argument advanced by researchers [12][14] is that by providing added flexibility, FACTS controllers can enable a line to carry power closer to its thermal rating. Mechanical switching needs to be supplemented by rapid-response power electronics. The reference [16] emphasized that FACTS is an enabling technology, and not a one-on-one substitute for mechanical switches.

The FACTS technology is not a single high-power controller, but rather a collection of controllers, which can be applied individually or in coordination with others to control one or more of the interrelated system parameters mentioned above [12]. A well-chosen FACTS controller can overcome the specific limitations of a designated transmission line or corridor. It is said that because all FACTS controllers represent applications of the same basic technology, their production can eventually take advantage of technologies scale. It is noted in [17] that just as the transistor is the basic element for a whole variety of microelectronic chips and circuits, the thyristor or high-power transistor is the basic element for a variety of high-power electronic controllers. The FACTS concepts are based on the substantial incorporation of power electronic devices and methods into the high-voltage side of the network, to make it electronically controllable. FACTS controllers aim at increasing the control of power flows in the high-voltage side of the network during both steady state and transient conditions [17]. The concept of FACTS as a total network control philosophy was introduced in 1988 by Dr. N. Hingorani [18]. .

Owing to many economical and technical benefits it promised, FACTS received the support of electrical equipment manufacturers, utilities, and research organizations around the world. This interest has led

to significant technological development of FACTS controllers [18] [19] [20]. Several kinds of FACTS controllers have been commissioned in various parts of the world [23] [24]. The most popular are load tap changers, phase-angle regulators, static VAR compensators, thyristor controlled series compensators, interphase power controllers, static compensators, and unified power flow controllers.

III. Model Design and Analysis.

This model is the shunt and series controllers of the UPFC for the control of voltage injection into power system in the events of fault transients. The FACTS controllers are configured to control the absorption or injection of energy into the system, in order to damp out the transient energy within a few microseconds of a fault current, preventing the onset of damaging current from reaching utility equipment, such as circuit breakers and surge arresters.

The proportional integral (PI) controller is a vital component of the UPFC control structure. The technique is to use the proportional integral (PI) controllers in the UPFC controllers (shunt and series controllers) to dynamically adjust the phase angle between the FACTS devices voltage source converters (VSCs) and the power system bus voltage in order to adaptively generate or absorb energy at the connection point during a fault transient. To achieve this, the strategy is to use the combination of the Phase Locked Loop (PLL) and the UPFC shunt and series PI controllers to generate pulse sequence that controls the magnetic coupling of the energy interchange between the FACTS devices and the power system.

Analysis of the fault current limiting effect of the UPFC is developed to explain the impact of limiting fault current at the fault point. The analysis given here shows the dynamics of the FACTS device series injected voltage in limiting the impact of the fault, having protecting key assets on the power transmission system. Actually what is happening between the FACTS devices and the power system is energy interchange. If this interchange between the power electronics and the power system can be adaptively controlled, the system can be made to react in the event of fault current hence limiting the fault current by quickly absorbing energy at the connection point.

Hence, the strategy adopted here is to use the PLL and the UPFC PI controllers to generate pulse sequence that controls the magnetic coupling of the energy interchange between the FACTS devices and the power system. Most of the injected voltage which is quadrature with the size current, emulates an inductive or a capacitive reactance in series with the transmission line. This emulated variable reactively inserted by the injected voltage source, influences the electric power flow through the transmission line.

IV. The UPFC Controller Model and Implementation

The UPFC is made up of two voltage source converters (VSCs) with semiconductor devices having turn off capability, sharing a common dc capacitor and connected to a power system through coupling transformers. The model of the UPFC is specified using a power balance equation that couples the shunt and series ac/dc converters through it common dc link, as well as through their physical system connections, as proposed in [20]. is expanded into the functional model as given in Figure 1.

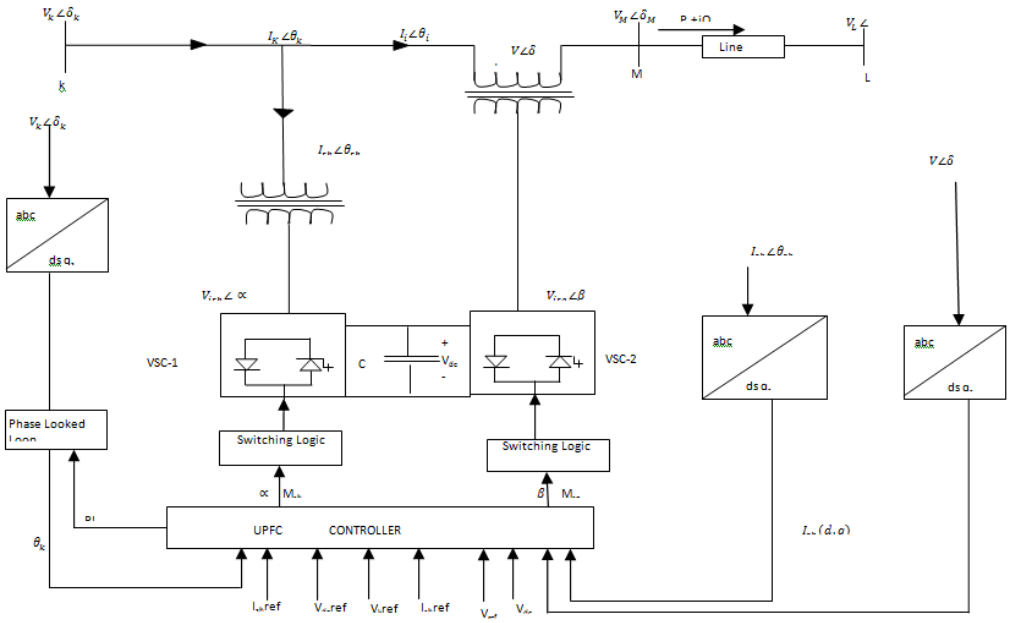

Figure 1: The UPFC Functional model

The main objective of the series converter is to produce an ac voltage of controllable magnitude and phase angle, and inject this voltage at fundamental frequency into the transmission line, exchanging real and reactive power at its ac terminals through the series connected transformer. The shunt converter provides the required real power at the dc terminals; thus, real power flows between the controller shunt and series ac terminals through the common dc link.

Based on the power balance technique proposed in [20] for a STATCOM mode,

$P_{ac} = P_{dc} + P_{losses}$ (1)

Thus, the three-phase instantaneous power flowing into the shunt converter from the ac bus, neglecting transformer losses and assuming fundamental frequency and balanced conditions, can be represented by

$P_{sh} = 3\, V_k I \cos(\delta_k - \theta_{sh})$ (2)

Where $V_k\angle\delta_k$ is the rms phasor of the sinusoidal sending-end voltage V_k (i.e at bus k) and $I_{sh}\angle\theta_{sh}$ is the rms phasor of the shunt converter's sinusoidal current. It can be observed that the instantaneous three-phase power is the same as the average power of a balanced system.

For the series branch, the three phase instantaneous power flowing into the series converter order fundamental frequency, balanced conditions is represented by

$P_{se} = 3\, V I_L \cos(\delta - \theta)$ (3)

Where $I_L\angle\theta_L$ is the r.m.s phasor value of the ac line current I_L,

and $V\angle\delta = V_k\angle\delta_k - V_m\angle\delta m$ is the rms phasor of the series converter's output voltage V_L.

It is important to point out that these phases are defined with respect to the system reference; however, in the UPFC controller implementation, the converter sinusoidal voltage V_{ish} is typically referred to the controller shunt or sending end bus voltage V_k:

$V_k = \sqrt{2}\, V_k Sin\,(\omega t + \delta_k)$

$$V_{ish} = \sqrt{2} V_{ish} Sin\left(\omega t + \underbrace{\delta_k + \Delta\propto}_{\alpha}\right) \quad (4)$$

For the series phasor voltage the controls designed in this work assuming that it is synchronized with respect to the receiving-end bus voltage V_L, i.e.,

$V_k = \sqrt{2} V_i Sin\,(wt + \delta_k)$

$$V_{ise} = \sqrt{2}\, V_{ise} Sin\left(wt + \underbrace{\delta_i + \Delta\beta}_{\beta}\right) \quad (5)$$

Considering series resistors R_{sh} and R_{se} (not indicated in figure1), AC losses in both converters can be modeled. DC losses may be represented with a resistor Rc = 1/Gc connected in shunt with the dc capacitor. The UPFC power balance of equation (1.1), assuming real power flow from shunt converter to the series converter may be given by

$$P_{sh} - P_{se} = V_{dc}\left(\underbrace{C\,\frac{dVdc}{dt}}_{I_{dc}}\right) + V_{dc}^2\, GC + 3(a_{sh} I_{sh})^2 R_{sh} + 3(a_{se} I_{se})^2 R_{se} \quad (6)$$

Where a_{sh} and a_{se} are the shunt and series transformers voltage ratios, and V_{dc} is the average dc capacitor voltage. Hence, from equation (2, 3 and 6), it follows that the UPFC dc voltage V_{dc} in the transient stability model can be defined by the following non linear differential equation:

$$\frac{\delta V_{dc}}{dt} = 3\frac{V_k I_{sh}}{C\, V_{dc}}\cos(\delta_k - \theta_{sh}) - 3\,\frac{V I_L}{C V_{dc}}\cos(\delta - \theta_L) - \frac{Gc}{C} V_{dc} - \frac{3 d_{sh}^2 I_{sh}^2}{C V_{dc}} R_{sh}$$

$$- 3\frac{d_{se}^2 I_{se}^2}{C V_{dc}}\, R_{se} \quad (7)$$

If ac losses represented by R_{sh} and R_{se} are neglected, equation (7) can be transformed into:

$$\frac{dV_{dc}}{dt} = 3\frac{V_k K_{sh}}{C\, d_{sh} X_{sh}} sin\,(\delta_k - \propto) - 3\,\frac{V K_{se}}{C d_{se} \times_{se}}\, sin\,(\delta - \beta) - \frac{Gc}{C} V_{dc} \quad (8)$$

Here, K_{sh} and K_{se} are defined based on a Fourier Analysis of the converter's output voltage V_{ish} and V_{ise}, respectively. Since V_{ish} and V_{ise} are the corresponding rms values, these can be expressed as

$$V_{ish} = \frac{1}{2\sqrt{2}}\, M_{sh}\, V_{dc} = K_{sh}\, V_{dc} \quad (9)$$

$$V_{ish} = \frac{1}{2\sqrt{2}}\, M_{se}\, V_{dc} = K_{se}\, V_{dc} \quad (10)$$

Where M_{sh} and M_{se} represent the amplitude modulation indices for the control (i.e firing) of the shunt and series converters, respectively.

V. Analysis of the Fault Current Limitation of UPFC device

The idea behind the destructive fault-current limitation concept is to minimize the voltage at the fault point through the action of the injected series voltage, V. This, in fact, is an extension of the Thevenin's prefault voltage concept at the fault point. Based on this, Figure 2 is used to present the analysis. For the case of a three-phase fault occurring at bus 3 (Figure 2), as it can be seen the contribution of the two independent loops L (left) and R (right) to the fault point. In fact, the series voltage will reduce the current contribution from the left AC system (E_i).

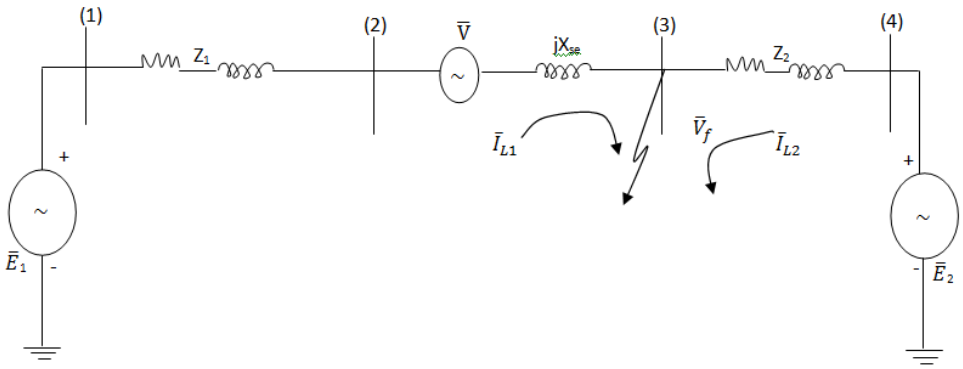

Figure 2: Series VSC converter seen as a fundamental frequency source for fault

This reduction will be more effective when the UPFC injects positive sequence voltages in opposition to the left equivalent source, which can be estimated in each operative condition. If it is intended to minimize the total current at the fault point, the series voltage injected must be in opposition to the prefault voltage at the fault point. As the voltage along the line has a smooth behaviour, it is not difficult to set values to cover some other cases of fault along the compensated line.

The left and right equivalent impedances, from the fault point up to each AC source, are defined as Z_L and Z_R, respectively. For a phase-to-ground fault, which is the case more likely to occur, to minimize the current contributions to the fault, a more careful analysis must be performed. Such an analysis can be done through phase or sequence components.

Thus, regarding the fault point considered in Figure 2 which can be located at any point along the line Z_2, and with the term X_{se} included within the equivalent impedance Z_L (left side), it can be established that

$$[E_1^1] = [E_1] + [V] \quad (11)$$

Under the absence of the fault, the line current in the system will be

$$[I_L] = [Z_L + Z_R]^{-1}[E_1^1 - E_2] \quad (12)$$

The pre-fault voltage at bus 3 can be expressed as

$$[V_3] = [E_2] + [Z_R][I_L] \quad (13)$$

Substituting (12) into (13) and calling M the matrix that represent the voltage divider, yields:

$$[V_3] = ([I] - [M])[E_2] + [M][E_1] + [M][V] \quad (14)$$

Where [I] represents the identity matrix. Also

$$[M] = [Z_R][Z_L + Z_R]^{-1} \quad (15)$$

In order to simplify (14) the first two terms (i.e those affected by E_1, E_2 without the effect of V) will be named as V_{uf} (uncompensated fault voltage), whereas the last term will be designated as V_{sc} (series compensated voltage at the fault point F). Thus, the compensated fault voltage (V_f) in (14), former V_3, becomes:

$$[V_f] = [V_{uf}] + [M][V] \quad (16)$$

To minimize V_f, the compensation term [M][V] has to be in opposition to V_{uf}, with the series voltage (V) being inserted at its maximum possible magnitude during fault period.

The contribution of the coupling effect of unaffected phases to the fault currents limitation has to be considered. The inductive effect of the unaffected phases is analyzed. Hence, if the product of the resulting impedance matrices in (16) were renamed as that shown in (17), where to simplify the analysis transposed lines are considered.

$$[M] = \begin{vmatrix} \propto & \beta & \beta \\ \beta & \propto & \beta \\ \beta & \beta & \propto \end{vmatrix} \quad (17)$$

Factors ∝, β are dependent on the equivalent impedance Z_L and Z_R and on the zero and positive sequence values which define the coupling effect between phases . The substitution of (17) into (16), yields:

$$\begin{bmatrix}\bar{V}_{fa}\\ \bar{V}_{fb}\\ \bar{V}_{fc}\end{bmatrix} = \begin{bmatrix}\bar{V}_{ufa}\\ \bar{V}_{ufb}\\ \bar{V}_{ufc}\end{bmatrix} + \begin{bmatrix}\propto & \beta & \beta\\ \beta & \propto & \beta\\ \beta & \beta & \propto\end{bmatrix} \begin{bmatrix}\bar{V}_a\\ \bar{V}_b\\ \bar{V}_c\end{bmatrix} \quad (18)$$

For instance, the corresponding terms affecting the fault point at phase "**a"**, are:

$$\bar{V}_{fa} = \bar{V}_{ufa} + \propto \bar{V}_a + \beta(\bar{V}_b + \bar{V}_c) \quad (19)$$

VI. Simulation And Result Evaluation

The Nigerian 330kV power system was used to simulate and assess the effectiveness of the UPFC in limiting fault currents in the system. The one line diagram of the 330kV system is noted and the system is modeled in MATLAB. The SIMULINK model of the 330kV power system is given in Figure 3.

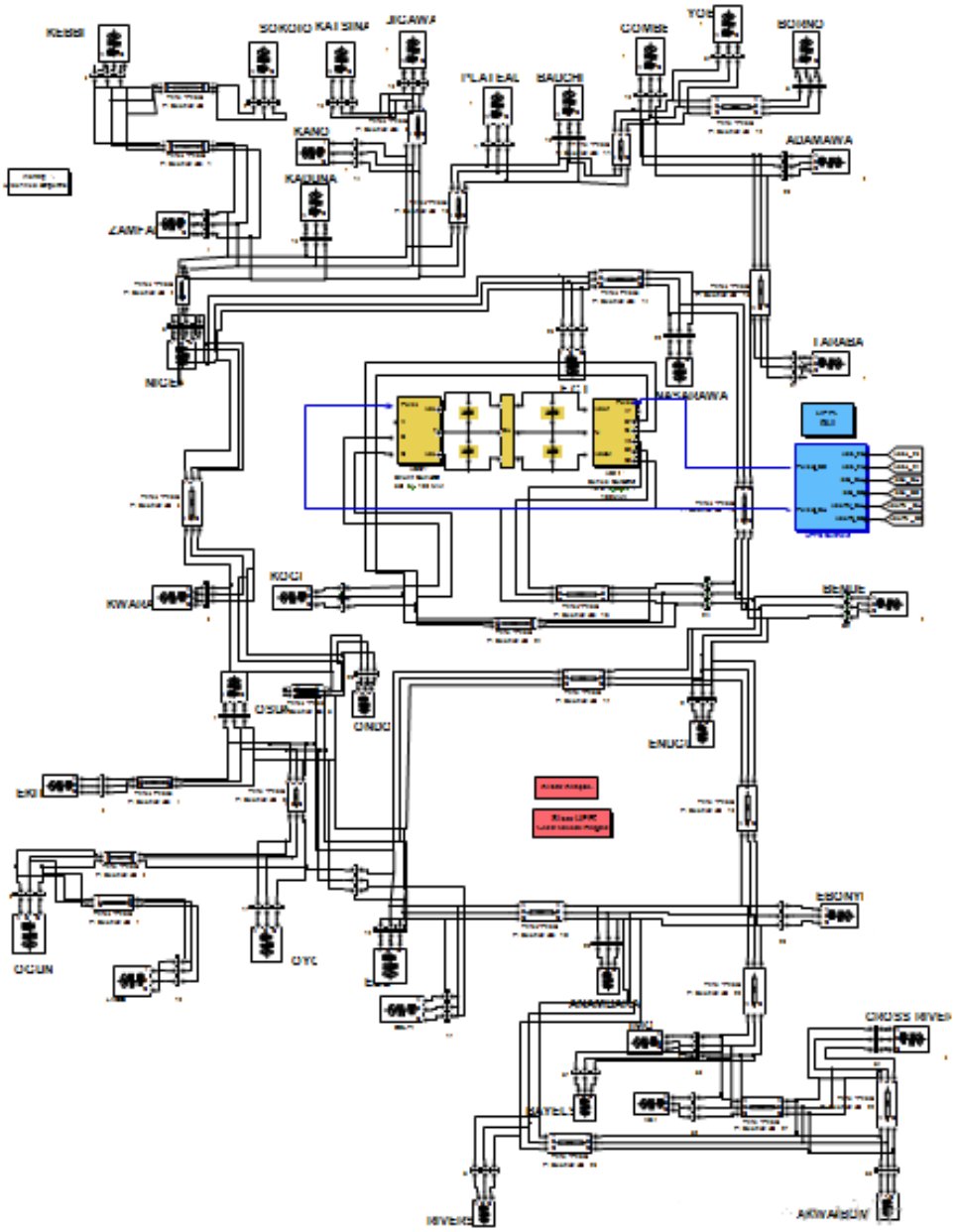

FIGURE 3: Simulink Model of The Nigerian 330kv Power System With UPFC Integrated For Protective Fault Current Limitation

Both the shunt and series converters (VSCI and VSC2) have PI (proportional integral) type of controllers that are the reference parameter values with those existing previously in the system. . As indicated, the PI parameters (k_p and k_i) are the input form of the MATLAB work space during the simulation as indicated

by the matrix blocks (k_p) and (k_i). These values are the input from the work space representing PI control parameters (k_p) (K_i) that have been obtained from the simulation of the network within the MATLAB process workspace. This enables the PI controller to send optimal control values to optimize the voltage injection by the UPFC during network disturbance.

VII. Evaluation of System Fault State Operation with the UPFC

System response to 3 phase fault is evaluated. 3-phase fault is induced in the power system. To simulate this in SIMULINK, three-phase fault block is connected at bus 25 (i.e at Kogi) as shown in Figure 1.3. The SIMULINK three-phase fault block is configurable. The fault level of this block can be programmed by adjusting the fault impedance (fault resistance). This is done using the properties page of the three-phase block. To simulate different levels of faults, the fault impedance is set to 1Ω, 0.1 Ω, 0.01 Ω, 0.001 Ω and 0.0001 Ω. It is important to note that the lower the fault resistance, the higher the fault MVA. This means higher maximum short-circuit current. Fault level is proportional to the reciprocal of the fault impedance. The UPFC fault current limitation action for different fault impedances is shown in Table 1.

Table 1: UPFC Fault Current Limitation action for different Fault Impedances

Fault Impedance Ω	**power System Fault-Current rose to (kA):**	**UPFC reduced fault current to (kA):**	**percentage Fault current reduction %**
1	16.5357	8.25	66.2856
0.1	28.2321	13.4464	61.1070
0.01	39.4732	18.2589	59.8640
0.001	50.8929	24.9643	55.3354
0.0001	68.4286	33.8571	53.68837
			Average reduction = 59.23%

The fault transition time of the SIMULINK three-phase fault block is set for 0.4 sec. The signal profile of the system response towards the 3-phase short-circuit current with the UPFC installed is shown in Figures 4 for fault impedances of 1 Ω..

Figure 4 gives the current signal profile without the UPFC installed. From Figure 4 it can be seen that the excessive short-circuit current is sustained form of fault inception (at t = 0.4 sec) onwards without protective limitation.

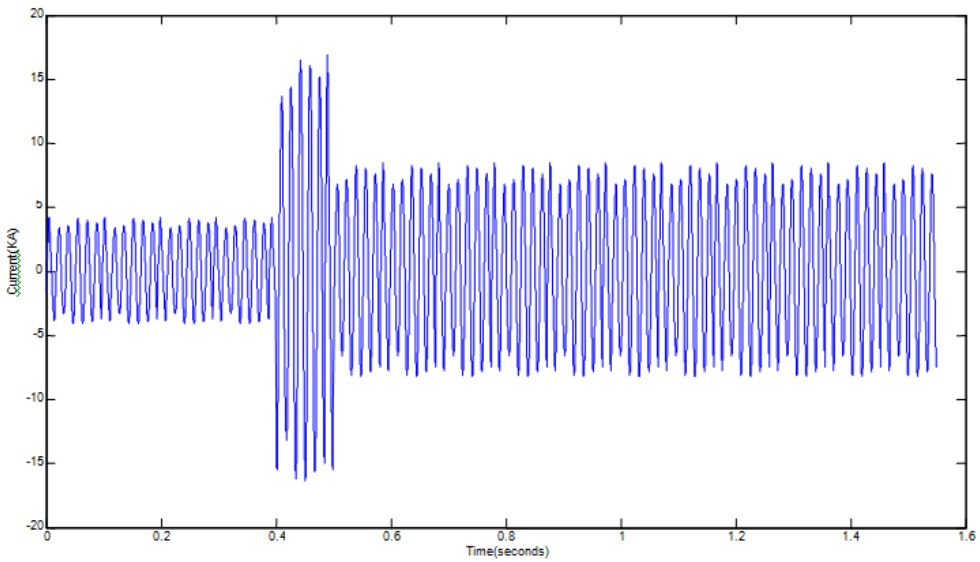

Figure: 4: Signal profile of system with UPFC installed for fault impedance of 1 OHMS

Referring to Figure 4 the steady state current level (peak-to-peak) is around 4.0357kA at fault state (fault transition system current rose to 16.5357kA. At t = 0.4988 sec the high current was reduced to 8.25kA as a result of the controlled voltage injection by the UPFC.

Before UPFC response:

Fault current above steady state current is 16.5357 – 4.0357 = 12.5kA, but

After UPFC response (i.e at t = 0.4988 sec):

Fault current above steady state is 8.25 – 4.0357 = 4.2143 kA.

This means that the UPFC reduced the short circuit current from 12.5kA to 4.2143kA. This represents a reduction of about 66.29% in relation to the peak-to-peak current value existing during the no fault condition.
For the other fault impedances of 0.1 Ω, 0.01 Ω, 0.001 Ω and 0.0001 Ω (Table 1) is made after the simulation in MATLAB for signal profile of the power system with UPFC installed. The average limitation of the fault current is estimated to be 59.23%. This shows a significant reduction of the excessive fault current. This significant reduction in the short-circuit current would be very important in the protection of existing transmission assets on the power system, especially circuit breakers.

VII. Comparison of the response time of the UPFC and the Circuit Breaker

Comparison is here made between the protection intervention response speed of the UPFC and that of the relay/circuit breaker pair.
Fault transition times of t = 0.4 sec, 0.5 sec, 0.6 sec, 0.7 sec and 0.8 sec with fault impedance of 1 Ω are used. These five fault scenarios are simulated with the UPFC installed in the network and with the UPFC not installed but replaced with relay/circuit breaker protection system.
Figures 5 gives the trip response of the relay/circuit breaker protection system for the 3-phase fault transition times of t = 0.4.
Figures 6 gives the protective limiting response of the UPFC for the same sequence of fault transition time.

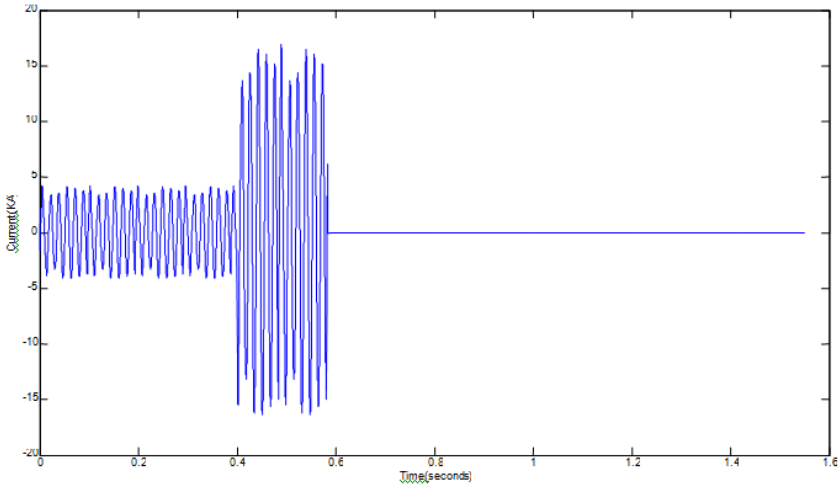

Figure 5: Signal profile of system with UPFC replaced with relay/circuit breaker protection for fault transition time of 0.4seconds

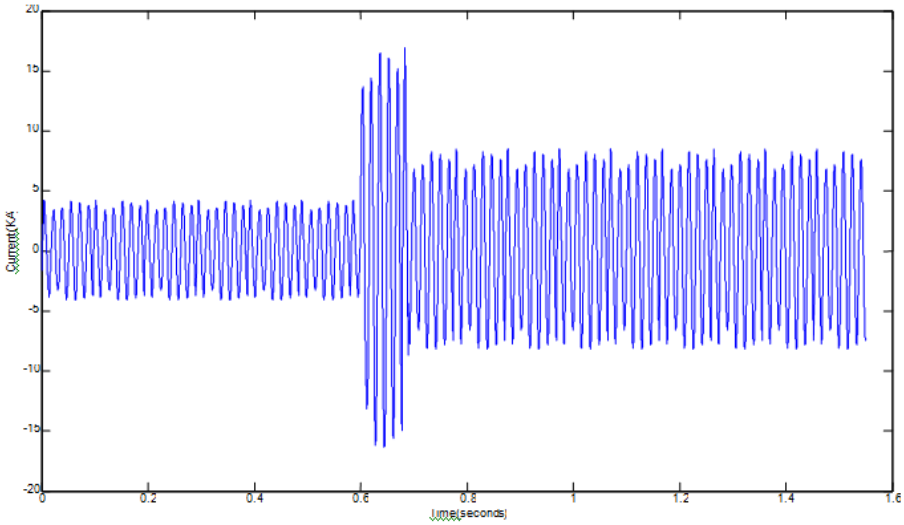

Figure 6: Signal profile of system with UPFC installed for fault transition time of 0.6seconds

The variations of the response of the circuit breaker and the UPFC are summarized in Table 2. The estimated average response time of the circuit breaker is 0.2143 sec, while that of the UPFC is 0.01922 sec. The difference in time response is 0.19503 sec and this represents a 91% difference. This means that the protective response of the facts device is faster than that of the relay/circuit breaker system by an average margin of 91%. This wide disparity in the response of these systems can be explained from the design, support systems, configuration (level of integration with the power system) and the materials used in the manufacture of these devices. The operation time of the current transformer (CT) associated with the operation of the relay/circuit breaker introduces unavoidable delay to the operation of this conventional protection system. This is coupled with the delay with the relay (especially for non solid state relays) plus the delay in the mechanical sub-assemblies that operate the breaker contacts. These are coupled together to introduce substantial delay compared to the fully solid state FACTS device. The FACTS device response is almost instantenous (with very negligible latenly), since the FACTS device is fully solid state. Furthermore, the FACTS device is fully coupled with the dynamics of the power system as electronic control system. The operation of the FACTS device does not depend on any mechanical action throughout its reaction sequence.

However, this evaluation does not suggest replacing the relay/circuit breaker with FACTS devices. What is meant to show is that, in the combination of FACTS and the conventional protection system (relay/circuit breaker), the FACTS device swings faster into action than the relay/circuit breaker. This helps to quickly limit the dangerous fault current to a level that reduces excessive stress on the circuit breaker. For this improved protection combination to be effective and still maintain the quality of the power supply (without service interruption) the speed of the FACTS device should be electronic. Furthermore, the reduction of the fault current by the UPFC might be to such a level that would not require the circuit breaker to react.

Table 2 Comparison of the fault clearing response time of the UPFC and the circuit breaker.

Fault transition time sec	UPFC	Relay/breaker trip time after fault occur (sec)	UPFC disposed time before response (sec)	Elapsed time before response(sec)
0.4	0.4988	0.5838	0.0988	0.1838
0.5	0.5960	0.723	0.096	0.223
0.6	0.6899	0.8279	0.0899	0.2279
0.7	0.7983	0.9503	0.0983	0.2503
0.8	0.8975	0.9865	0.0975	0.1865

VIII. Conclusion

The paper developed the digital model of the Nigerian 330kV transmission system, employing UPFC as a protection device. This is done to illustrate the protective fault current limitation capacity of the UPFC on high voltage systems. The results of the simulations carried out show the effectiveness of the UPFC in reducing the level of fault currents. The current profile of the power system was observed when it was operated with UPFC and without UPFC under different short-circuit scenarios. The estimated 59.23% reduction of the level of fault current by the UPFC represents a very significant reduction of excessive current signal.

Importantly, the impact of the high current reduction capability of the UPFC has significant implications for the protection of assets on the power system especially circuit breakers. It was shown that UPFC reduced the high short-circuit current from a value above the interruption capacity of circuit breakers installed in the system to a value very much below the short circuit interruption capacity of the circuit breakers by an appreciable margin. This would not only protect the circuit breakers from explosion, but would also help to increase the life expectancy of circuit breaker contacts between overhaul. This means reduction on maintenance runs of circuit breakers, busbars, arresters etc. It means more money being saved and higher returns on investments on transmission assets on the 330kV system.

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